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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,418	11/30/2001	James R. Hsia	A-69632/ESW/WEN	4072

7590 06/09/2003

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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 06/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/007,418	HSIA ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

Applicants' claim for domestic priority from provisional application is approved.

Information Disclosure Statement

Information disclosure statements filed 25 March 2002 as paper number two and 1 April 2003 as paper number three have been considered by examiner. Signed and initialed copies of each are attached hereto.

Specification

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-6, 10-16, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callison et al (US Patent # 6,370,611) and Yao et al (US Patent # 6,021,464).

With respect to independent claims 1 and 6, at least one memory matrix unit having at least one memory subsystem including a memory array having a plurality of

memory "devices" arranged in a plurality of banks, each device (inherently) capable of storing data therein is disclosed by Callison et al in figure 1, #104. The separation of the memory into "banks" or devices" is discussed in column 7, lines 44-65, for example. The management unit coupled to [the] at least one memory matrix unit and to the data network to interface between the memory matrix unit and the data network is shown in figure 1, #106.

The difference between the instant claims and Callison et al is the recitation of a cache couple to the memory controller, the cache having stored therein one or more copies of a Data Allocation Table (DAT) adapted to describe data stored in the memory devices.

Yao et al disclose a data allocation table in figure 1, #252. As seen in the figure, and further discussed in columns 3 and 4, the data is "described" by its disk, block, size, and file.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Callison et al and Yao et al before him/her, to utilize the data allocation table of Yao et al in the system of Callison et al because the data allocation table of Yao et al allows data to be re-allocated automatically onto disk device, irrespective of how the data was stored when it was first received, as discussed by Yao et al in column 6, lines 60-65.

With respect to claims 5 and 10, Callsion et al disclose the memory devices comprising RAM is figure 1, #104.

With respect to claim 11, Callison et al disclose a non-volatile storage device to provide "backup" of data stored in the memory matrix unit in figure 1, #118. Callison et al disclose the memory #104 as being a cache and a RAID. By definition, a cache holds the same contents as it's "main" memory, which is, in Callison et al, the disk device of figure 1, and is therefore, a "backup" copy in NV memory of same.

With respect to claim 12, the NV storage unit comprising a magnetic disk drive is disclosed by Callison et al in figure 1, #118.

With respect to claim 13, the NV storage unit comprising a plurality of hard disk drives being connected in a RAID configuration to provide mirrored copies of data in at least one memory matrix unit is disclosed by Callison et al in column 3, lines 38-39, and column 4, lines 51-52. A mirror is inherently a copy, and this is provided in Callison et al by the cache RAID.

With respect to claim 14, Callison et al disclose a non-volatile storage unit comprising a plurality of hard disk drives, wherein the hard disk drives are connected in a RAID level 0 configuration to reduce the time to backup data in at least one memory matrix unit is disclosed in column 3, lines 38-39. A RAID level 0 configuration is merely striping, and, calling this a RAID is technically a misnomer because there is no redundancy provided, although examiner recognizes that it is an accepted term of the art. Striping is discussed by Callison et al in column 1, lines 62-65.

With respect to claim 15, Callison et al disclose the hard drives comprising a hard drive adapted to create a "continuous backup" of data in at least one memory matrix unit on a periodic basis. This appears to be contradictory, as continuous backup isn't

continuous if it is only periodically performed. Nonetheless, this is, by definition, cache coherency in a hierarchical storage system. If the RAID/cache is a cache, which it is, as discussed supra, then it must be kept coherent with the "main memory" of the system, in this case the disk drives in figure 1, #118. Coherency is inherent – whether it is write-back or write-through, for example, the data must remain the same, otherwise every access to a same location will produce a different result, thereby rendering the storage useless.

With respect to claim 16, Callsion et al disclose an "off-line" storage in figure 1, #118.

With respect to claim 22, the data network being based on a physical wire connection is disclosed by Callison et al in figure 1, #108, for example.

Claims 2-4 and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callison et al (cited supra), Yao et al (cited supra), and Chen et al (US Patent #4,901,203).

The combination of Callison et al and Yao et al disclose the claimed subject matter upon which the instant claimed subject matter depends, as discussed supra with respect to the claims upon which the instant claims depend.

The difference between the combination of Callison et al and Yao et al is the recitation of multiple ports to enable the memory controller/network to access different devices in different banks simultaneously, such as writing data to one array while reading data from another, simultaneously.

Chen et al disclose these features in column 3, lines 10-15, as memory banks being independently accessible and parallel.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention, having the teachings of Callison et al, Yao et al, and hen et al before him/her, to utilize the multi-ported memory of Chen et al in the system of Callison et al and Yao et al, because the multiported design provides a high performance and balanced memory organization with sufficient bandwidth to support simultaneous high-speed CPU and I/O operations, as discussed by Chen et al in column 3, lines 20-25.

Claims 17-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Callison et al (cited supra), Yao et al (cited supra), and Jardine et al (US Patent # 6,195,754).

The combination of Callison et al and Yao et al disclose the claimed subject matter upon which the instant claimed subject matter depends, as discussed supra with respect to the claims upon which the instant claims depend.

The difference between the combination of Callison et al and Yao et al is the recitation with respect to claim 17 of an uninterruptible power supply (UPS) configured to supply power to at least one management unit, at least one memory matrix unit, the non-volatile storage unit, and the of-line storage unit from an electrical power line, and, in the event of a variation in power from the electrical power line, to provide power from a battery; with respect to claim 18, wherein the UPS being configured to transmit a signal to the management unit on variation of power from the electrical power line exceeding a first predetermined amount; with respect to claim 19, at least one

management unit further configured, on variation of power from the electrical power line exceeding a second predetermined amount, to signal users of the memory system in the data network and perform a controlled shutdown of the system; with respect to claim 20, upon restoration of power to the electrical power line, to restore the contents of at least one memory matrix unit from the backup copy of the memory matrix stored in the NV storage unit, reactivate the memory matrix as primary memory, reactivate other memory matrices as secondary memories if previously configured as such, and reactivate the NV storage unit as a secondary memory, thereby returning the memory system to normal operating condition; and with respect to claim 21, the at least one management unit being configured, upon restoration of power from the electrical power line, if the NV storage unit is unavailable, to restore at least one memory matrix unit directly from another backup copy of the memory matrix unit stored in removable storage media in an off-line storage unit.

Jardine et al disclose, with respect to claim 17, an uninterruptible power supply (UPS) configured to supply power to at least one management unit, at least one memory matrix unit, the non-volatile storage unit, and the of-line storage unit from an electrical power line, and, in the event of a variation in power from the electrical power line, to provide power from a battery in the Abstract and in figure 2; with respect to claim 18, wherein the UPS being configured to transmit a signal to the management unit on variation of power from the electrical power line exceeding a first predetermined amount, which is a first period of time, in the Abstract and in figure 2; with respect to claim 19, at least one management unit further configured, on variation of power from

the electrical power line exceeding a second predetermined amount, which is a second period of time, in the Abstract and figure 2, to signal users of the memory system in the data network and perform a controlled shutdown of the system (Abstract), which is inherent in that if the system is not powered up, it is unavailable to the users, an therefore signals them of it's status; with respect to claim 20, upon restoration of power to the electrical power line, to restore the contents of at least one memory matrix unit from the backup copy of the memory matrix stored in the NV storage unit, reactivate the memory matrix as primary memory, reactivate other memory matrices as secondary memories if previously configured as such, and reactivate the NV storage unit as a secondary memory, thereby returning the memory system to normal operating condition is disclosed in column 2, lines 13-18; and with respect to claim 21, the at least one management unit being configured, upon restoration of power from the electrical power line, if the NV storage unit is unavailable, to restore at least one memory matrix unit directly from another backup copy of the memory matrix unit stored in removable storage media in an off-line storage unit is disclosed in column 2, lines 13-18 as "bootstrap[ping]". Please also refer to the discussion of coherency in a hierarchical memory system with respect to claim 15.

Therefore, it would have been obvious tone of ordinary skill in the art at the time of the invention, having the teachings of Callsion et al, Yao et al, and Jardine et al before him/her, to utilize the UPS system of Jardine et al in the system of Callison et al and Yao et al, because the UPS system of Jardine et al because there is a need for a system to approximate its ability to ride through a power outage of indeterminate length

and to effect a switch to a memory hold-up model as that ability is exhausted by continuing power outage, as disclosed by Jardine et al in column 6, lines 1-6.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 703.306.5903. The examiner can normally be reached on 9-4-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703.308.1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703.305.3719 for regular communications and 703.305.3719 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.3900.

Christian P. Chace
DS/cpc
June 3, 2003

Donald Sparks
Supervisory Patent Examiner
Art Unit 2187

L Number	Hits	Search Text	DB	Time stamp
1	1174	((713/300) or (713/340)).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:29
2	914	(((713/300) or (713/340)).CCLS.) and UPS	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:29
3	2	(((713/300) or (713/340)).CCLS.) and UPS and (power adj variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:41
4	0	(((713/300) or (713/340)).CCLS.) and (uninterruptible adj power) and (power adj variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:42
5	2	(((713/300) or (713/340)).CCLS.) and (uninterruptible adj power) and (power adj3 variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:02
6	1	("5928368").PN.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:06
7	360	((714/14) or (714/22)).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:06
8	22	(((713/300) or (713/340)).CCLS.) and (power adj4 variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:08
9	15	(((713/300) or (713/340)).CCLS.) and (power adj4 variation) and backup	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:09
10	1	(((713/300) or (713/340)).CCLS.) and (power adj4 variation) and (backup adj3 memory)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:10
11	0	(((713/300) or (713/340)).CCLS.) and (power adj4 variation) and (backup adj3 copy)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:10
12	10	(power adj4 variation) and (backup adj3 copy)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:13
13	25	(power adj4 change) and (backup adj3 copy)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:22
14	5	(power adj4 alter$4) and (backup adj3 copy)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 09:22

US-PAT-NO: 6104810

DOCUMENT-IDENTIFIER: US 6104810 A

TITLE: Pseudorandom number generator with backup and restoration capability

---------- KWIC ---------

Brief Summary Text - BSTX (7):

Random number generators can be grouped into two types: true random and pseudorandom. True random number generators are based on some physical noise source of random information, such as alpha particles, output of a zener diode, power supply voltage variations, etc. The generator may use this random noise directly or may use it to control an oscillator. For example, U.S. Pat. No. 4,905,176 to R. A. Schulz, entitled "Random Number Generator Circuit", derives randomness from noise variations in the power supply voltage; these variations are used to control the frequency of a free-running oscillator.

Detailed Description Text - DETX (64):

The handling of S, T, and ps is the same for any reset, including the special reset issued by the microcode during the handling of errors. But the effect of the reset action on these registers depends on mode bit 902. In crypto module normal mode (bit 902 is zero), S and T are restored from battery backup copies in nonvolatile storage (step 510) and the value in ps is ignored. In crypto module test mode (bit 902 is one), S, T and ps are all set to zero.

US-PAT-NO: 5007082

DOCUMENT-IDENTIFIER: US 5007082 A

TITLE: Computer software encryption apparatus

---------- KWIC ---------

Brief Summary Text - BSTX (11):

In a presently preferred environment, the computer system has a processor for operating on data comprising arrangements of binary digits. The computer system has a power-on routine for causing the processor to scan a predetermined range of memory location addresses for instructions after power-on. The system includes a means for enabling the processor to communicate with the data storage media comprising program means for reading and writing data to a fixed data storage medium and to a removable data storage medium. The data security system of the invention comprises a security program disposed within the predetermined range of memory location addresses scanned by the power-on routine. The security program attaches itself at the BIOS level during the power-on routine and automatically alters the program means for reading and writing data to the removable data storage medium. The security program is capable of transforming data communicated between at least one of the fixed and removable data storage media and the processor. The transformation is conducted so that data stored on the one data storage media is represented using a different arrangement of binary digits than is used when the data is operated upon by the processor. Because the data is stored

in a different
arrangement of binary digits, the data will be virtually unintelligible when
operated upon by a processor in a computer system which does not have the
invention's decryption capability.

Detailed Description Text - DETX (37):
From the foregoing it will be seen that the present invention provides an
encryption and decryption system which is automatically installed during the
power-on self-test routine and is therefore quite difficult for the user to
defeat. The encryption and decryption takes place in direct response to the
BIOS level floppy diskette controller interrupt. The encryption and decryption
routines are thus automatically invoked at a primitive level below the disk
operating system kernel. This has the advantage of automatically encrypting
the floppy diskette directory and file allocation table, so that even the
manner in which information is stored on the diskette is altered so that
ordinary diskette copy and directory listing routines will not work. Backup
copies on floppy diskette of data stored on the hard disk using disk backup
commands will be similarly encrypted. By being specifically attached to the
diskette read and write sequence, read and write operations to the hard disk
are not affected. Thus the integrity of the data stored on the hard disk is
retained.

Claims Text - CLTX (10):
said security program means including an encryption BIOS program and a
vector table altering program, said vector table altering program being
automatically invoked during said power-on routine to alter said interrupt
vector table to substitute said encryption BIOS program for

at least a portion
of said second BIOS input/output program without altering
said first BIOS
input/output program;

L Number	Hits	Search Text	DB	Time stamp
1	1174	((713/300) or (713/340)).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:29
2	914	(((713/300) or (713/340)).CCLS.) and UPS	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:29
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4	0	(((713/300) or (713/340)).CCLS.) and (uninterruptible adj power) and (power adj variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:42
5	2	(((713/300) or (713/340)).CCLS.) and (uninterruptible adj power) and (power adj3 variation)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/06/02 08:42

714/14.22

L Number	Hits	Search Text	DB	Time stamp
16	17866	((707/2) or (707/10) or (707/202) or (707/204) or (707/205) or (709/201) or (709/213) or (709/217) or (709/220) or (709/223) or (710/22) or (711/104) or (711/112) or (711/114) or (711/147) or (711/156) or (711/162) or (711/170) or (711/173) or (714/6) or (714/47) or (714/52) or (714/758) or (714/759) or (714/769) or (714/770) or (714/773) or (714/777)).CCLS.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 16:53
17	4	((707/2|707/10|707/202|707/204|707/205|709/201|709/213|709/217|709/220|709/223|710/22|711/104|711/112|711/114|711/147|711/156|711/162|711/170|711/173|714/6|714/47|714/52|714/758|714/759|714/769|714/770|714/773|714/777)).CCLS. and (multi$5 adj ports) and (alloc$5 adj table) and (network adj interface) and ((parallel or simultaneous) adj access)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 16:54
18	6	(multi$5 adj ports) and (alloc$5 adj table) and (network adj interface) and ((parallel or simultaneous) adj access)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 17:00
19	3	(("6370611") or ("5708769") or ("6021464")).PN.	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 17:00
20	10	(multi$5 adj ports) and (alloc$5 adj table) and ((parallel or simultaneous) adj access)	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 17:05
21	6	(multi$5 adj ports) and (alloc$5 adj table) and RAID	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 17:08
22	100	(alloc$5 adj table) and RAID	USPAT; US-PGPUB; EPO; JPO; IBM_TDB	2003/05/29 17:08